AMENDMENTS TO THE CLAIMS

1-26 (Cancelled)

27. (Previously Presented) A semiconductor package comprising:

a paddle having an upper surface;

a plurality of leads arranged adjacent the paddle, at least some of the leads each having a lower surface and a lead lock comprising at least one element selected from the group of at least one locking lug, at least one disk-shaped protrusion, at least one dimple, inclined side walls having an increased width defined therebetween in an upward direction, a bent, partially etched inner end portion, at least one protrusion at the lower surface, and at least one partially etched portion at the lower surface;

a semiconductor chip having a lower surface and mounted on the paddle;

conductive wires each electrically connecting respective ones of the leads to the semiconductor chip; and

a resin encapsulant defining a bottom surface and at least partially encapsulating the semiconductor chip, the lead lock of each of the leads, and the conductive wires, wherein a portion of the lower surface of each of the leads is exposed at the bottom surface of the encapsulant.

28. (Previously Presented) The semiconductor package of Claim 27 further comprising:

a plurality of solder balls, each of the solder balls being attached to the lower surface of a respective one of the leads and serving as an external input/output terminal.

29. (Previously Presented) The semiconductor package of Claim 27 further comprising a plating layer applied to the lower surface of each of the leads.

30. (Previously Presented) The semiconductor package of Claim 27 wherein the lower surface of the semiconductor chip is attached to the upper surface of the paddle by a thermally conductive adhesive layer which is covered by the encapsulant.

31. (Previously Presented) The semiconductor package of Claim 27 wherein the paddle is generally flat and includes a partially etched portion which extends about the periphery thereof and is covered by the encapsulant.

32. (Currently Amended) A semiconductor package comprising:

a paddle having an upper surface;

a plurality of leads arranged adjacent the paddle, at least some of the leads each having a lower surface**, an upper surface** and a lead lock comprising at least one disk-shaped protrusion **which is partially defined by the upper surface of the lead and includes a bottom surface positioned between the upper and lower surfaces of the lead**;

a semiconductor chip having a lower surface ~~and mounted on the paddle~~, ~~wherein the lower surface of the semiconductor chip~~ **which** is attached to the upper surface of the paddle;

conductive wires each electrically connecting respective ones of the leads to the semiconductor chip; and

a resin encapsulant defining a bottom surface and at least partially encapsulating the semiconductor chip, the lead lock of each of the leads, and the conductive wires, wherein a portion of the lower surface of each of the leads is exposed at the bottom surface of the encapsulant.

33. (Previously Presented) The semiconductor package of Claim 32 further comprising:

a plurality of solder balls, each of the solder balls being attached to the lower surface of a respective one of the leads and serving as an external input/output terminal.

34. (Previously Presented) The semiconductor package of Claim 32 further comprising a plating layer applied to the lower surface of each of the leads.

35. (Previously Presented) The semiconductor package of Claim 32 wherein the lower surface of the semiconductor chip is attached to the upper surface of the paddle by a thermally conductive adhesive layer which is covered by the encapsulant.

36. (Previously Presented) The semiconductor package of Claim 32 wherein the paddle is generally flat and includes a partially etched portion which extends about the periphery thereof and is covered by the encapsulant.

37. (Previously Presented) A semiconductor package comprising:

a paddle having an upper surface;

a plurality of leads arranged adjacent the paddle, at least some of the leads each having a lower surface and a lead lock comprising inclined side walls having an increased width defined therebetween in an upward direction from the lower surface;

a semiconductor chip having a lower surface and mounted on the paddle;

conductive wires each electrically connecting respective ones of the leads to the semiconductor chip; and

a resin encapsulant defining a bottom surface and at least partially encapsulating the semiconductor chip, the lead lock of each of the leads, and the conductive wires, wherein a portion of the lower surface of each of the leads is exposed at the bottom surface of the encapsulant.

38. (Previously Presented) The semiconductor package of Claim 37 further comprising:

a plurality of solder balls, each of the solder balls being attached to the lower surface of a respective one of the leads and serving as an external input/output terminal.

39. (Previously Presented) The semiconductor package of Claim 37 further comprising a plating layer applied to the lower surface of each of the leads.

40. (Previously Presented) The semiconductor package of Claim 37 wherein the lower surface of the semiconductor chip is attached to the upper surface of the paddle by a thermally conductive adhesive layer which is covered by the encapsulant.

41. (Previously Presented) The semiconductor package of Claim 37 wherein the paddle is generally flat and includes a partially etched portion which extends about the periphery thereof and is covered by the encapsulant.